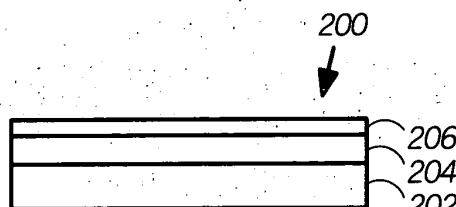


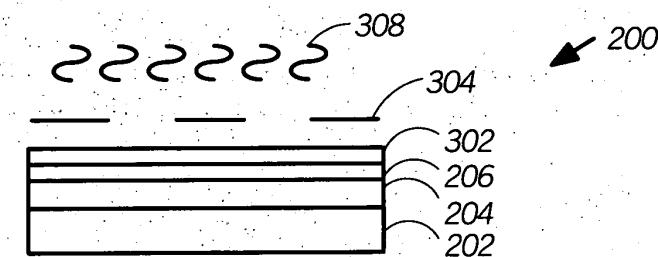
FIG. 1

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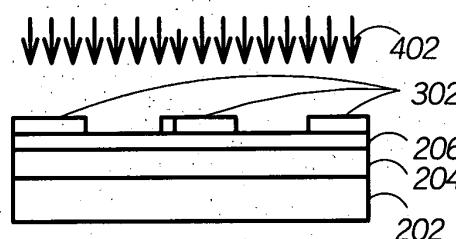
SOI WAFER-START

FIG. 2



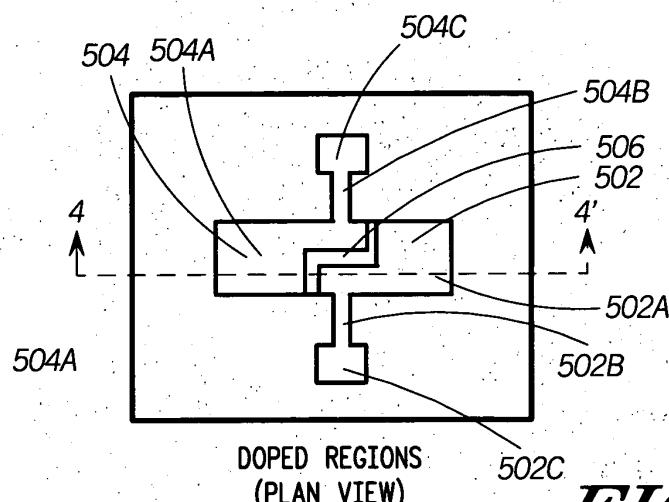
1ST RESIST EXPOSURE
(FOR DOPING)

FIG. 3



DOPING STEP

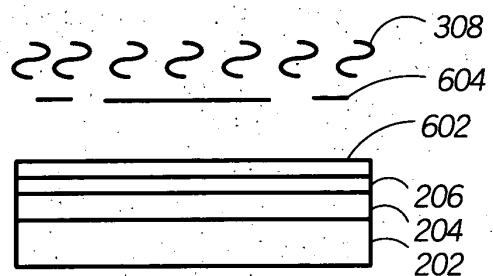
FIG. 4



DOPED REGIONS
(PLAN VIEW)

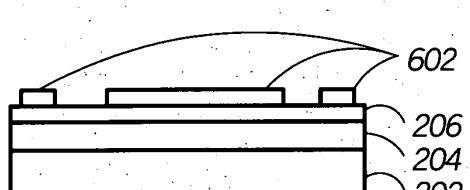
FIG. 5

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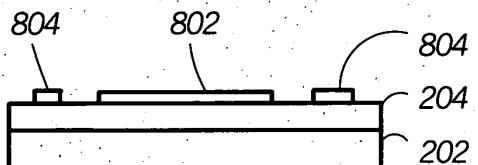
2ND RESIST EXPOSURE
(FOR SILICON ETCH)

FIG. 6



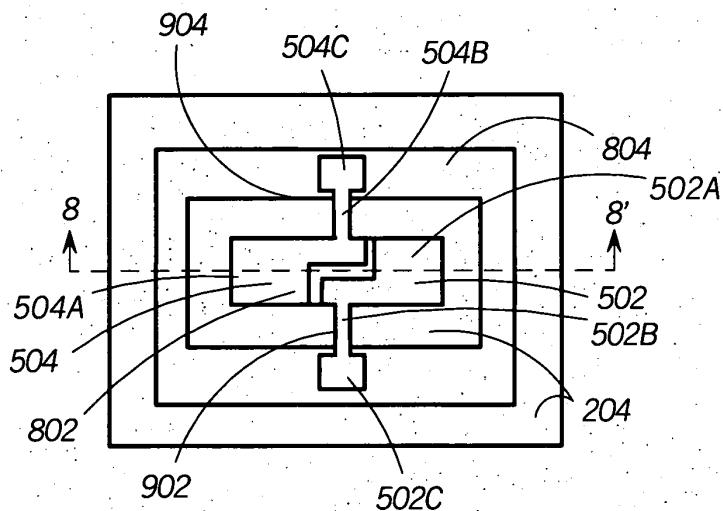
DEVELOPED RESIST

FIG. 7



ETCHED SILICON LAYER
SECTIONAL ELEVATION

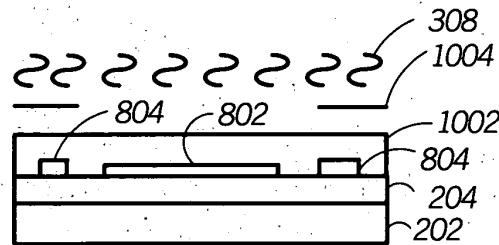
FIG. 8



ETCHED SILICON-PLAN VIEW

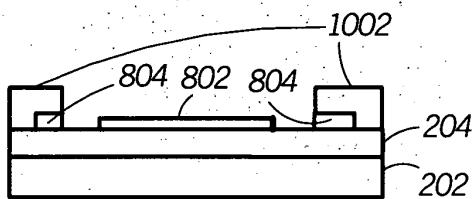
FIG. 9

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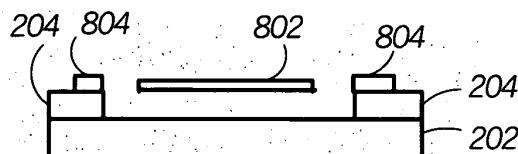
3RD RESIST EXPOSURE
(FOR SiO₂ ETCH)

FIG. 10



DEVELOPED RESIST

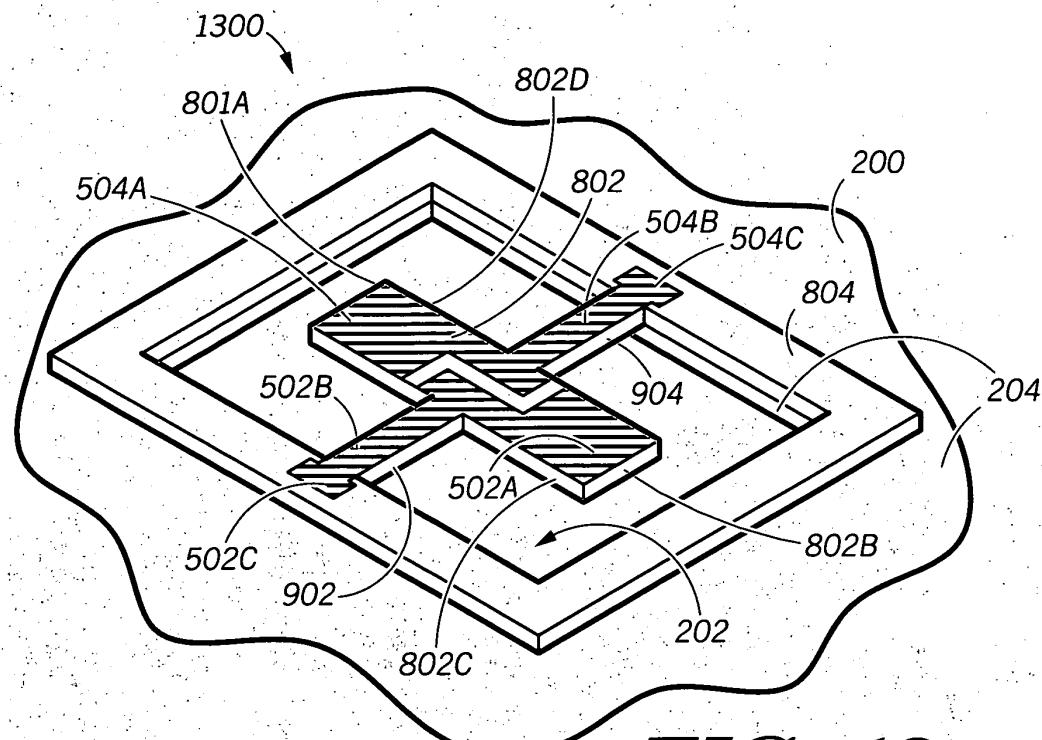
FIG. 11



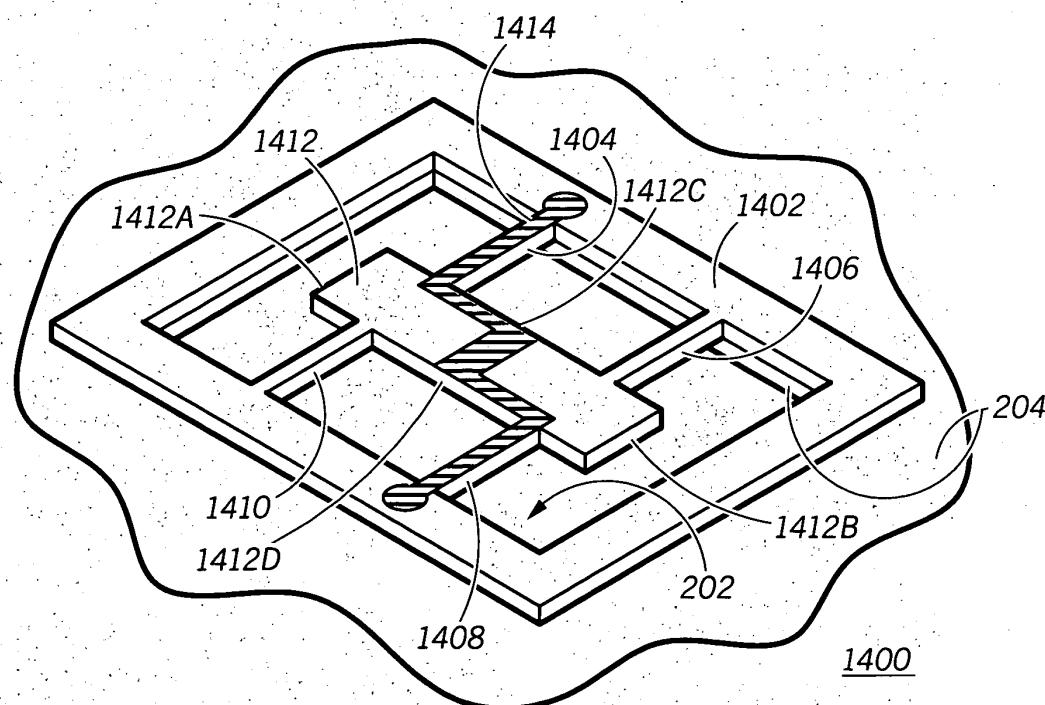
AFTER SiO₂ ETCH

FIG. 12

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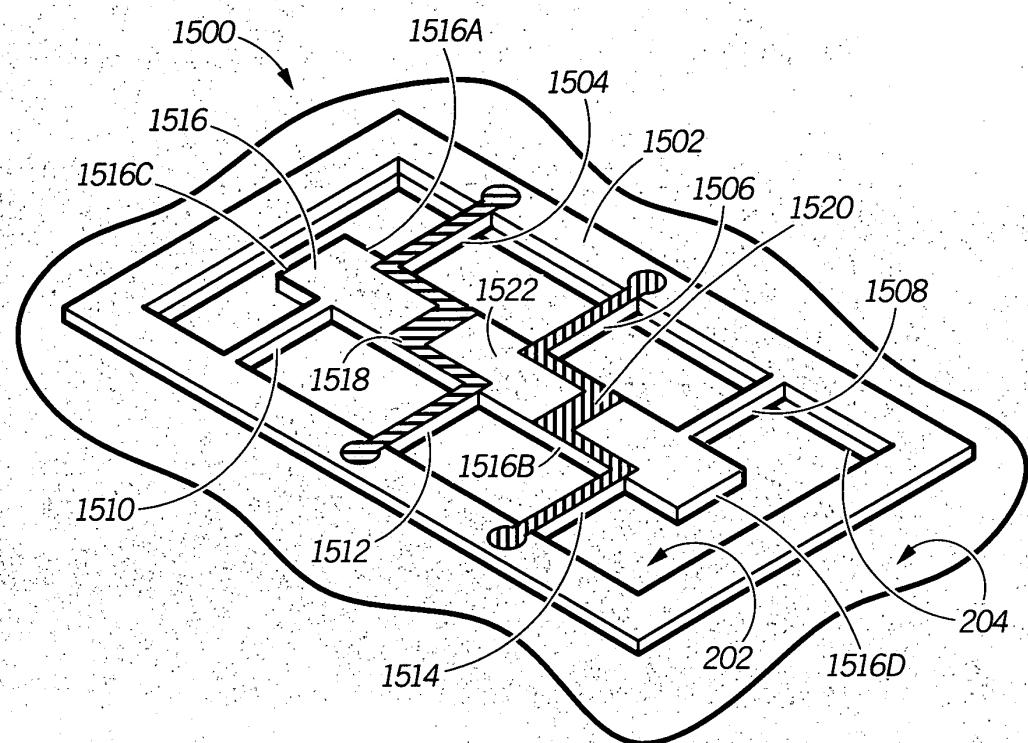


FIG. 15

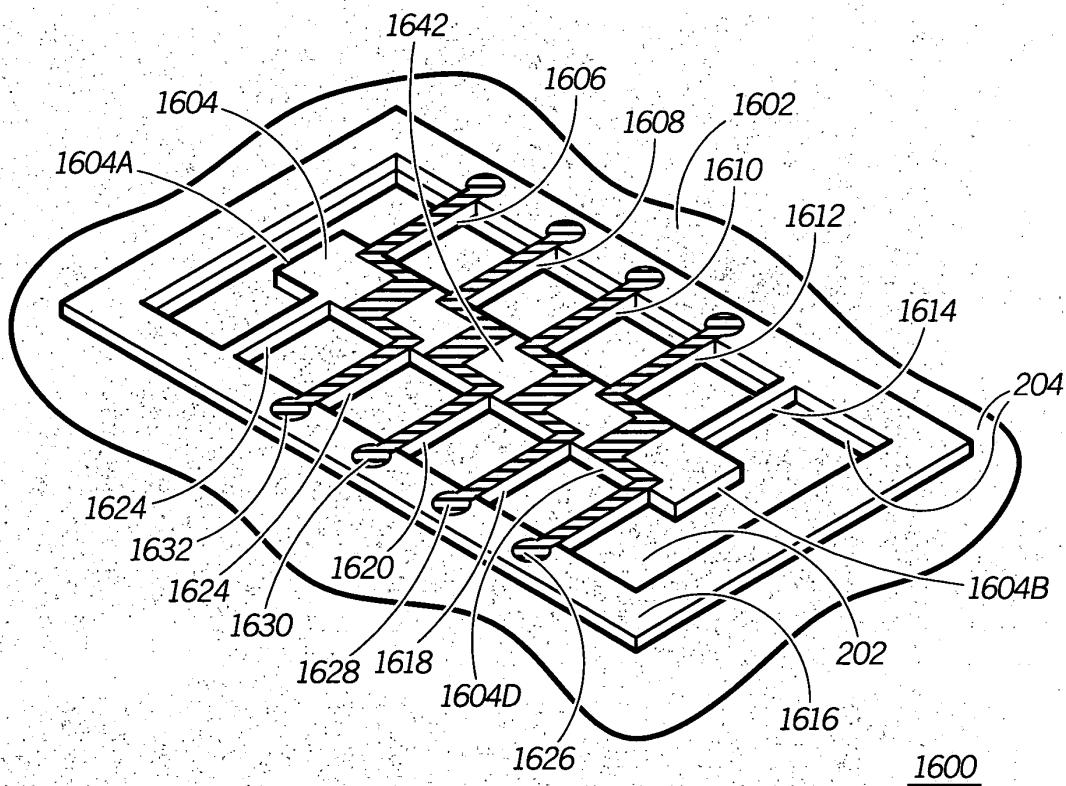


FIG. 16

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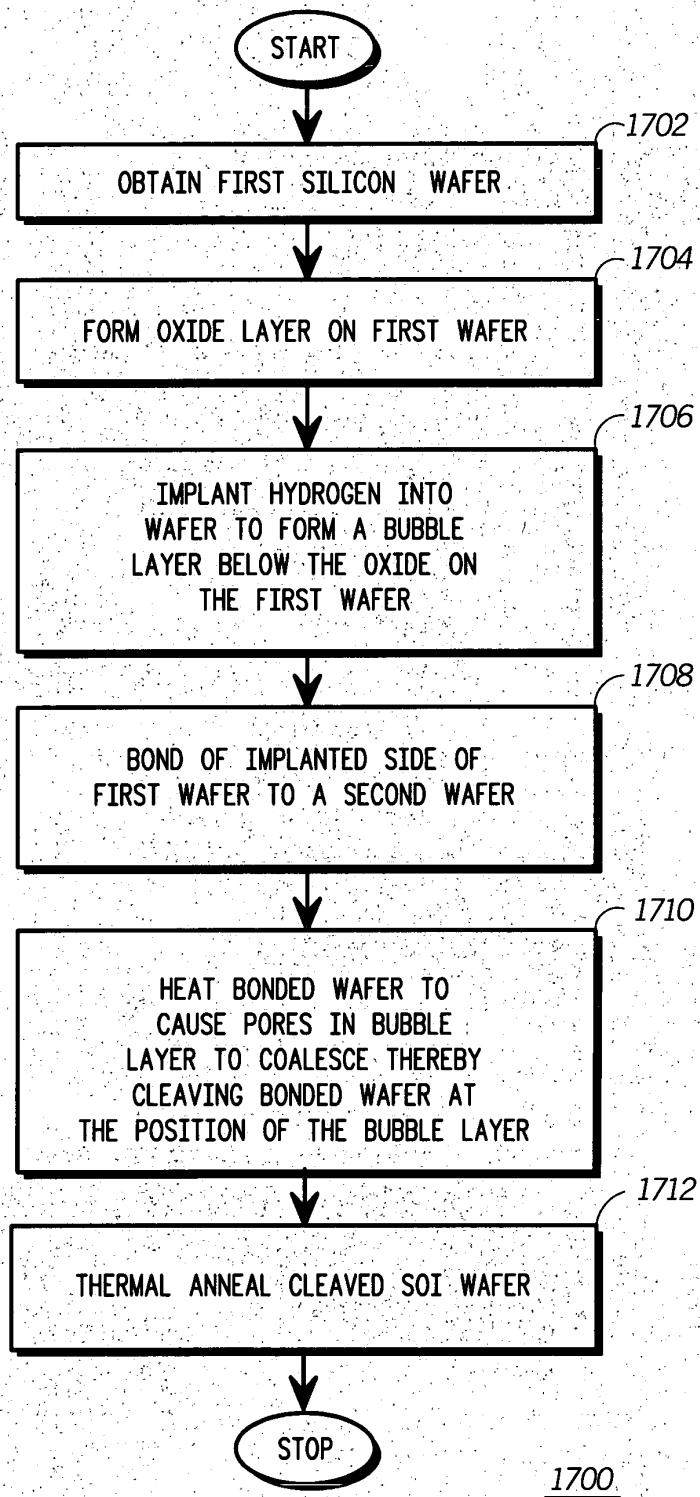


FIG. 17

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FIG. 18

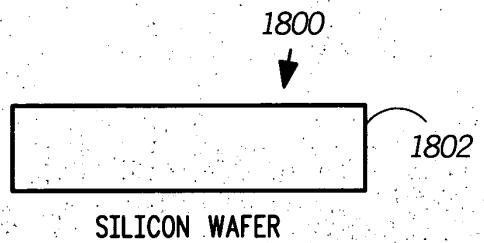


FIG. 19

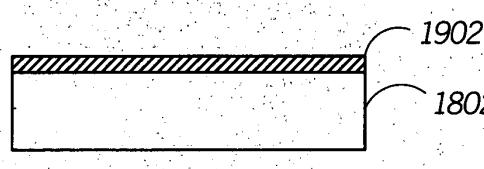


FIG. 20

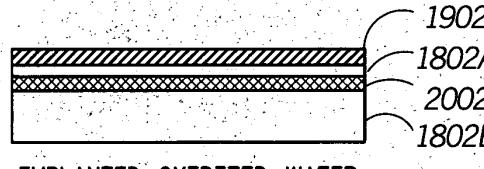


FIG. 21

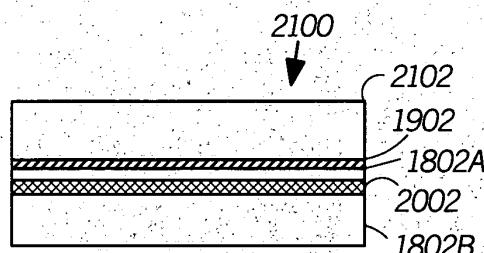
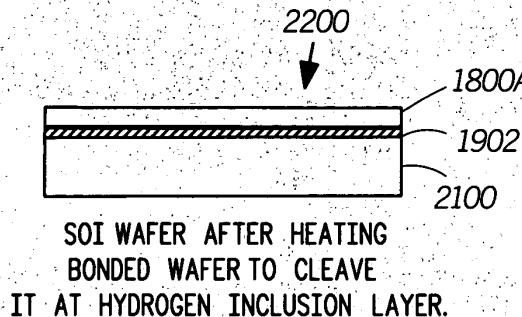


FIG. 22



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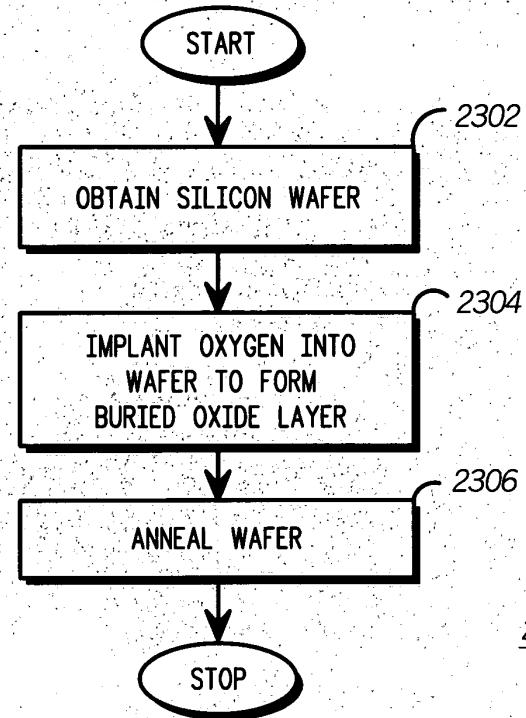


FIG. 23

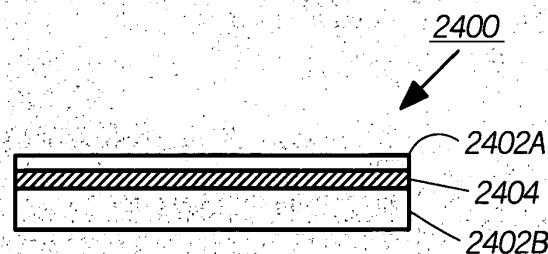


FIG. 24

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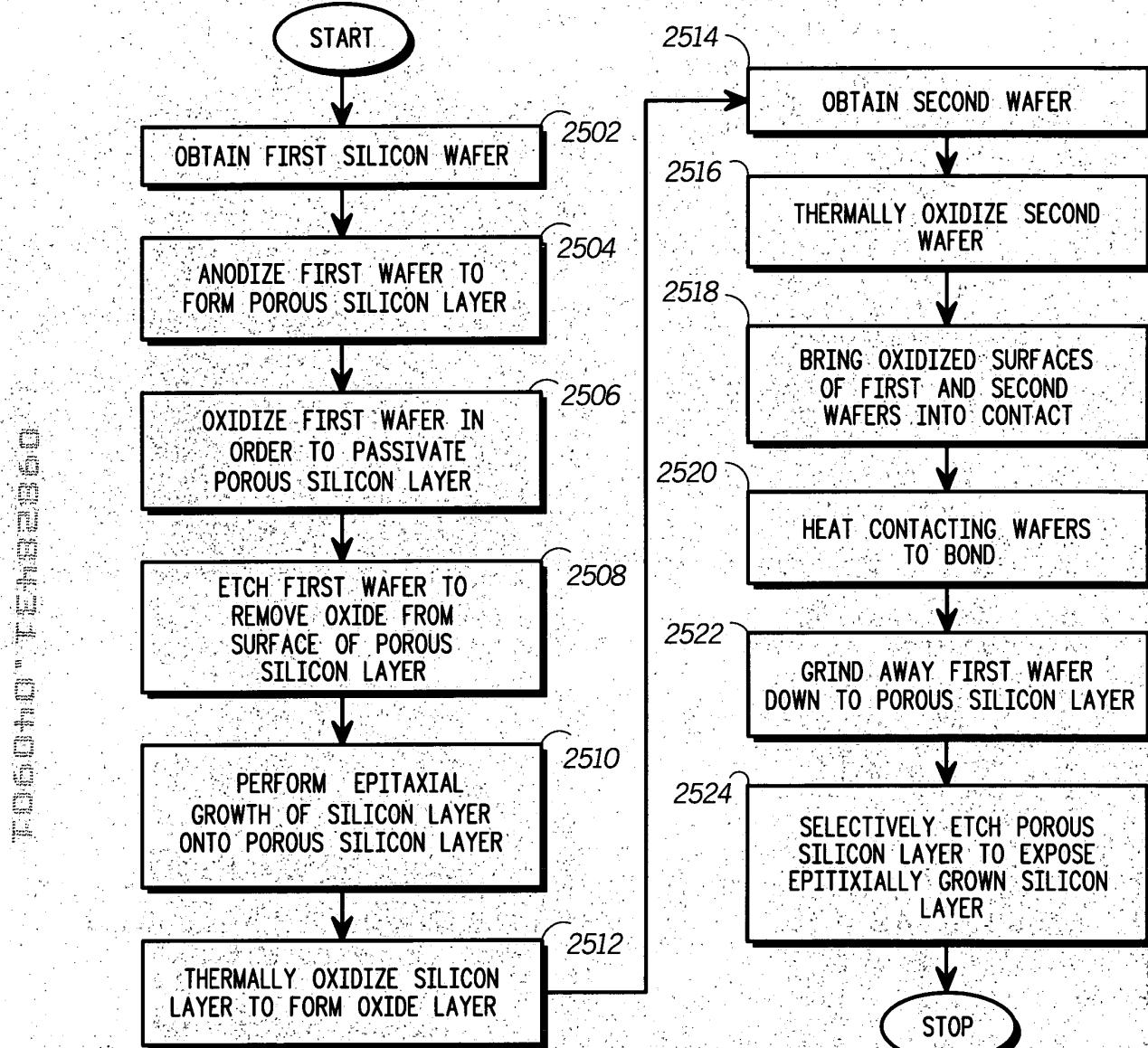


FIG. 25

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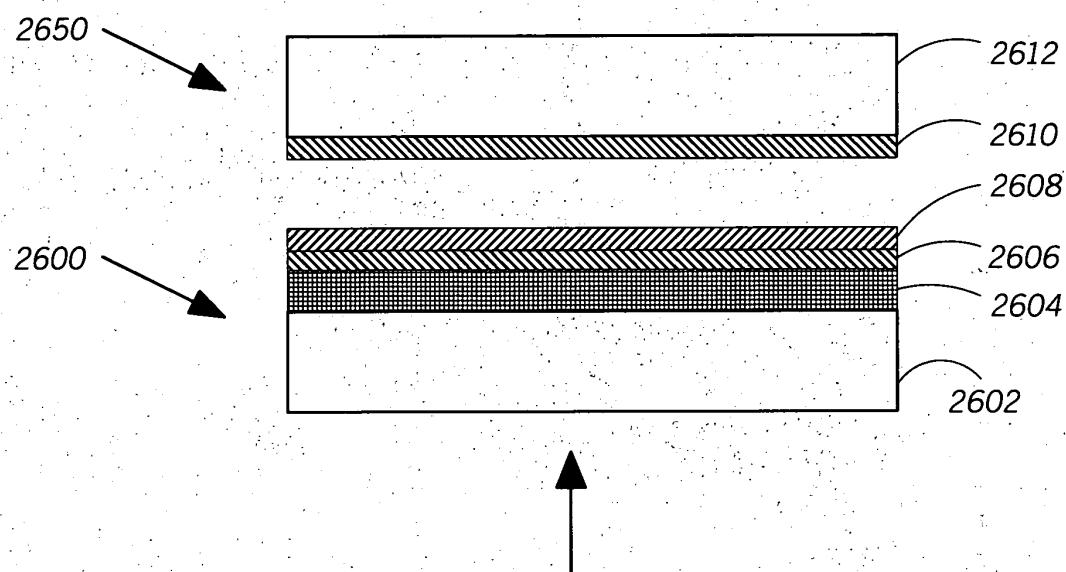


FIG. 26

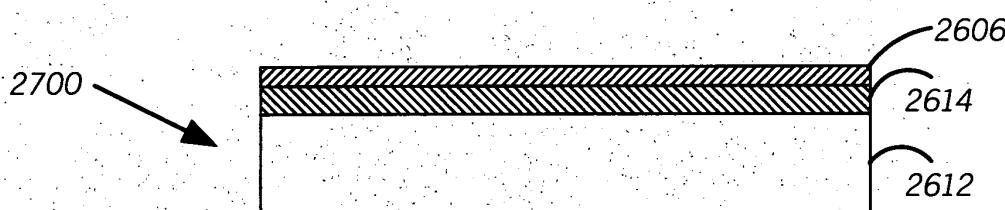


FIG. 27

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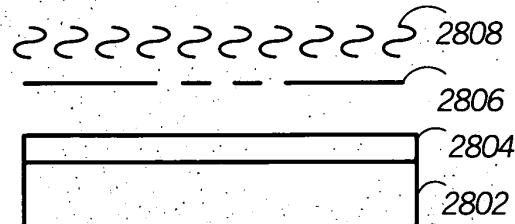


FIG. 28

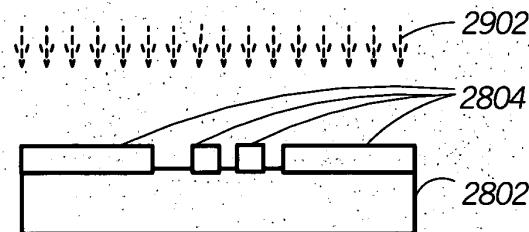


FIG. 29

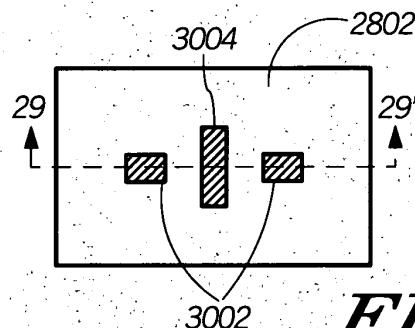


FIG. 30

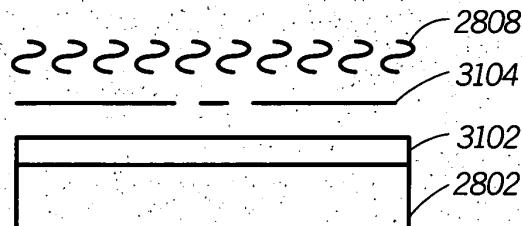


FIG. 31

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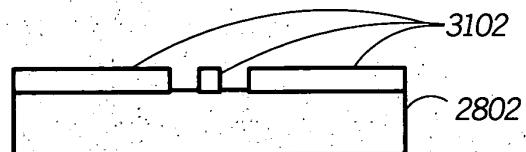


FIG. 32

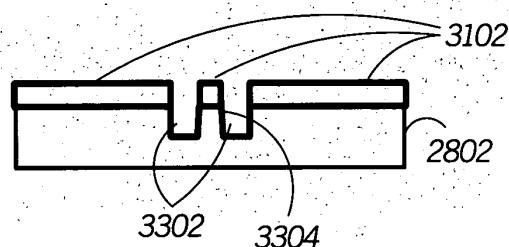


FIG. 33

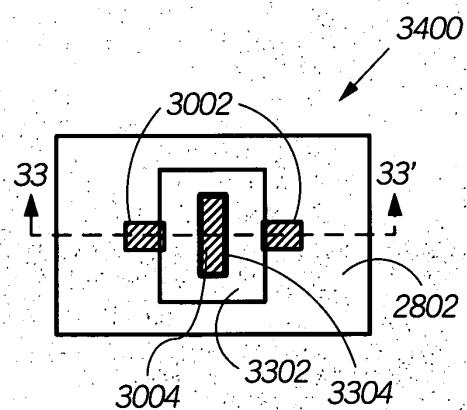


FIG. 34

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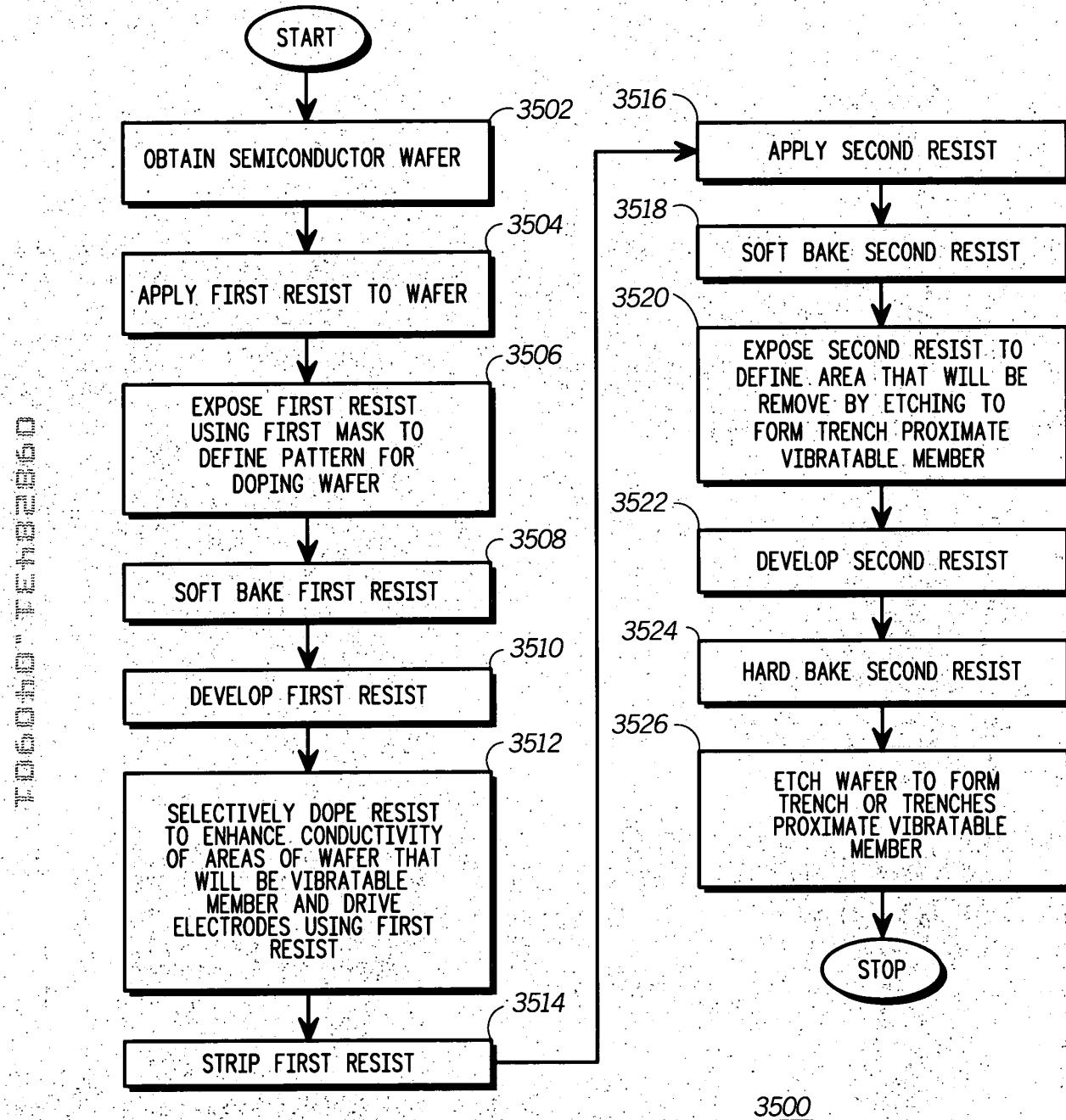


FIG. 35

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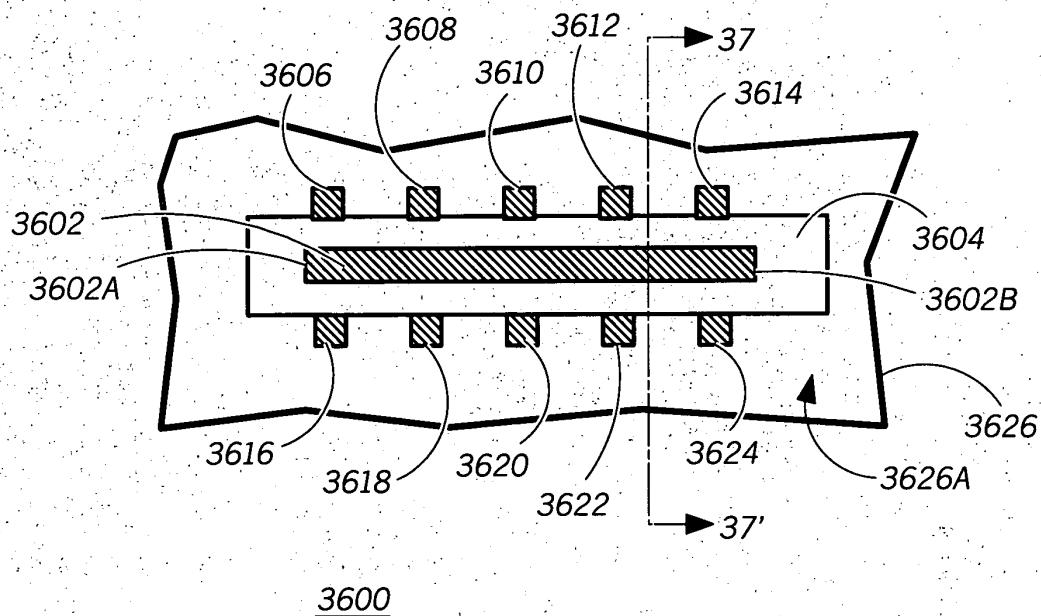


FIG. 36

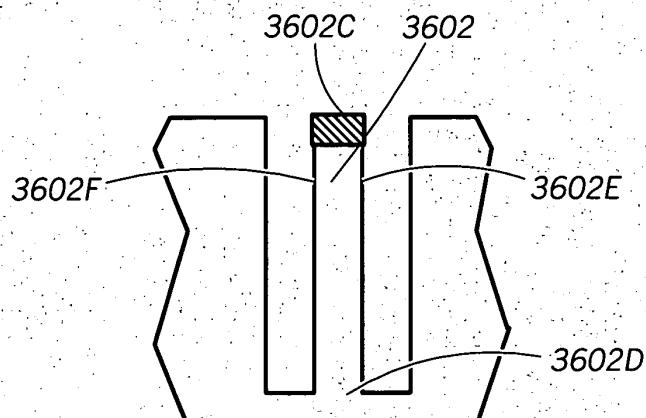


FIG. 37

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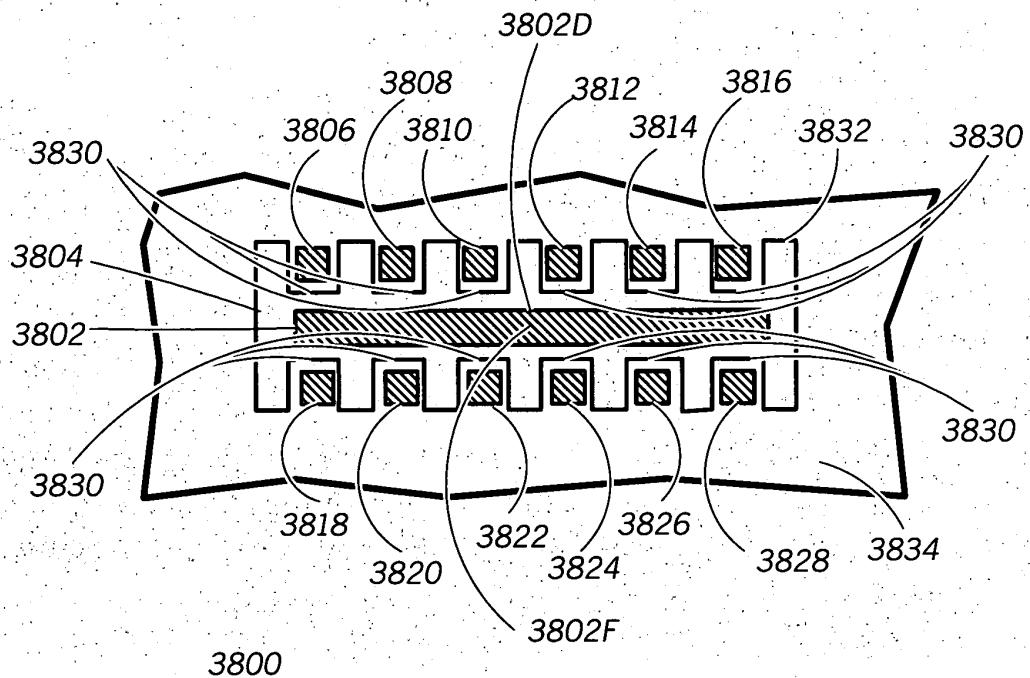


FIG. 38

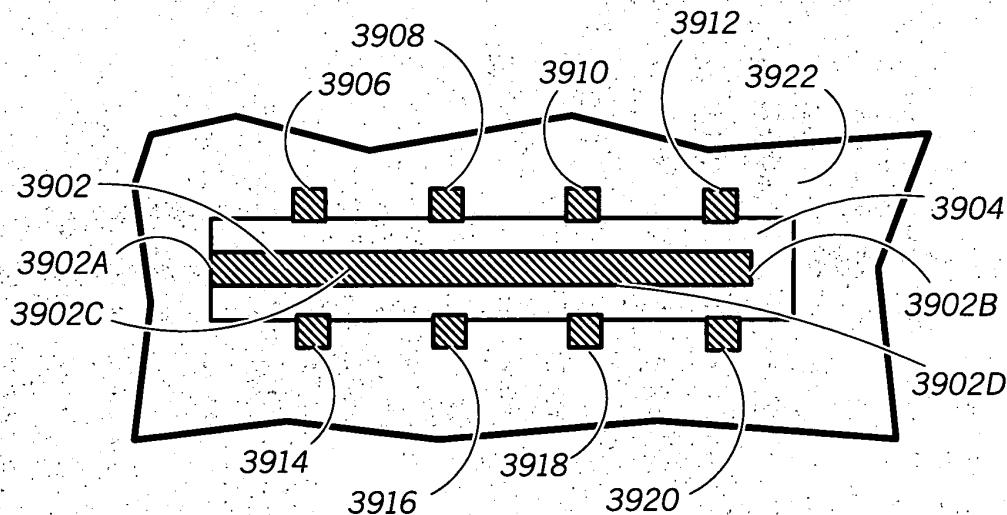


FIG. 39

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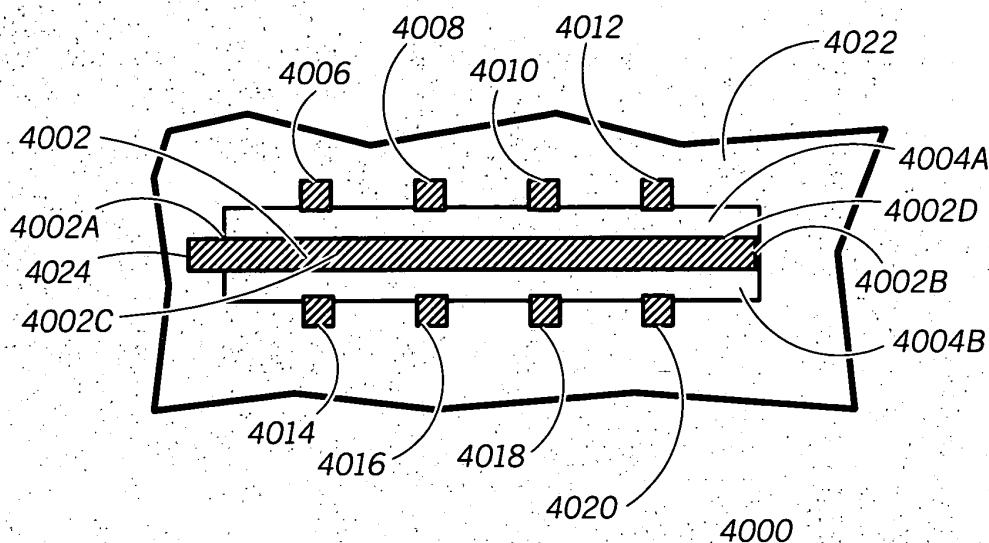


FIG. 40

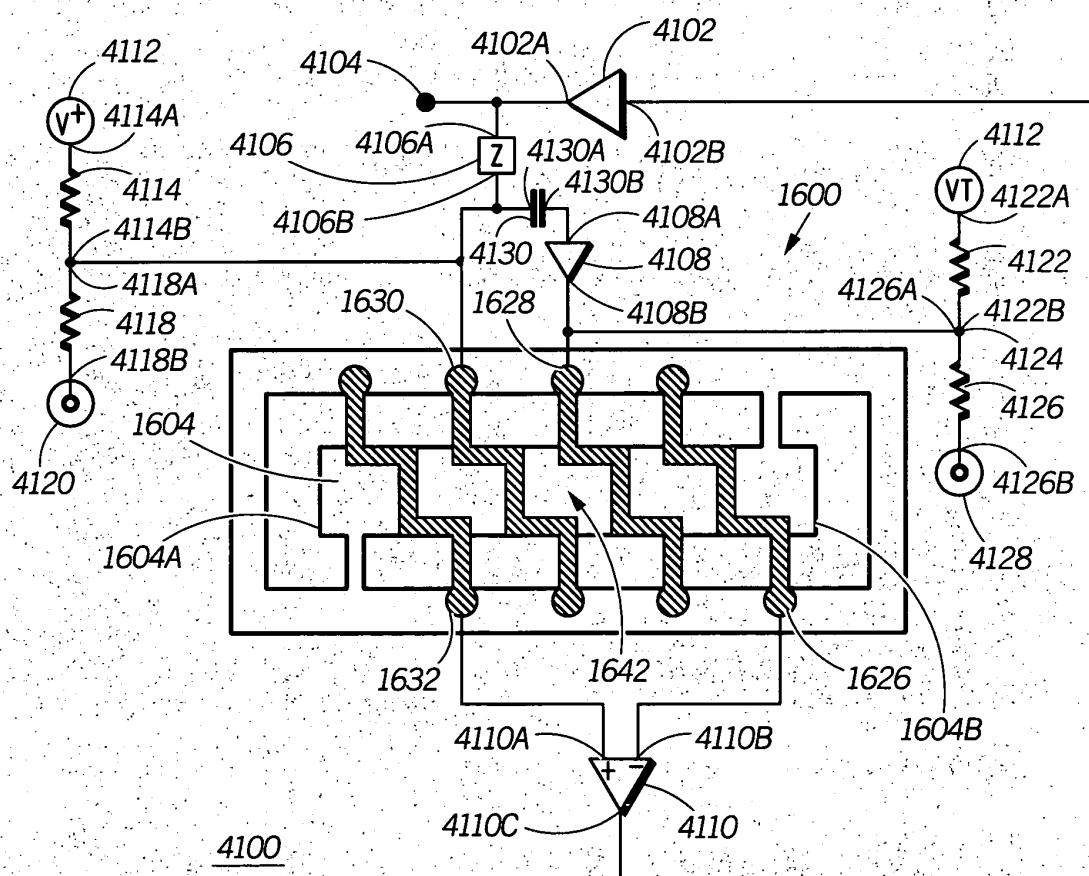


FIG. 41

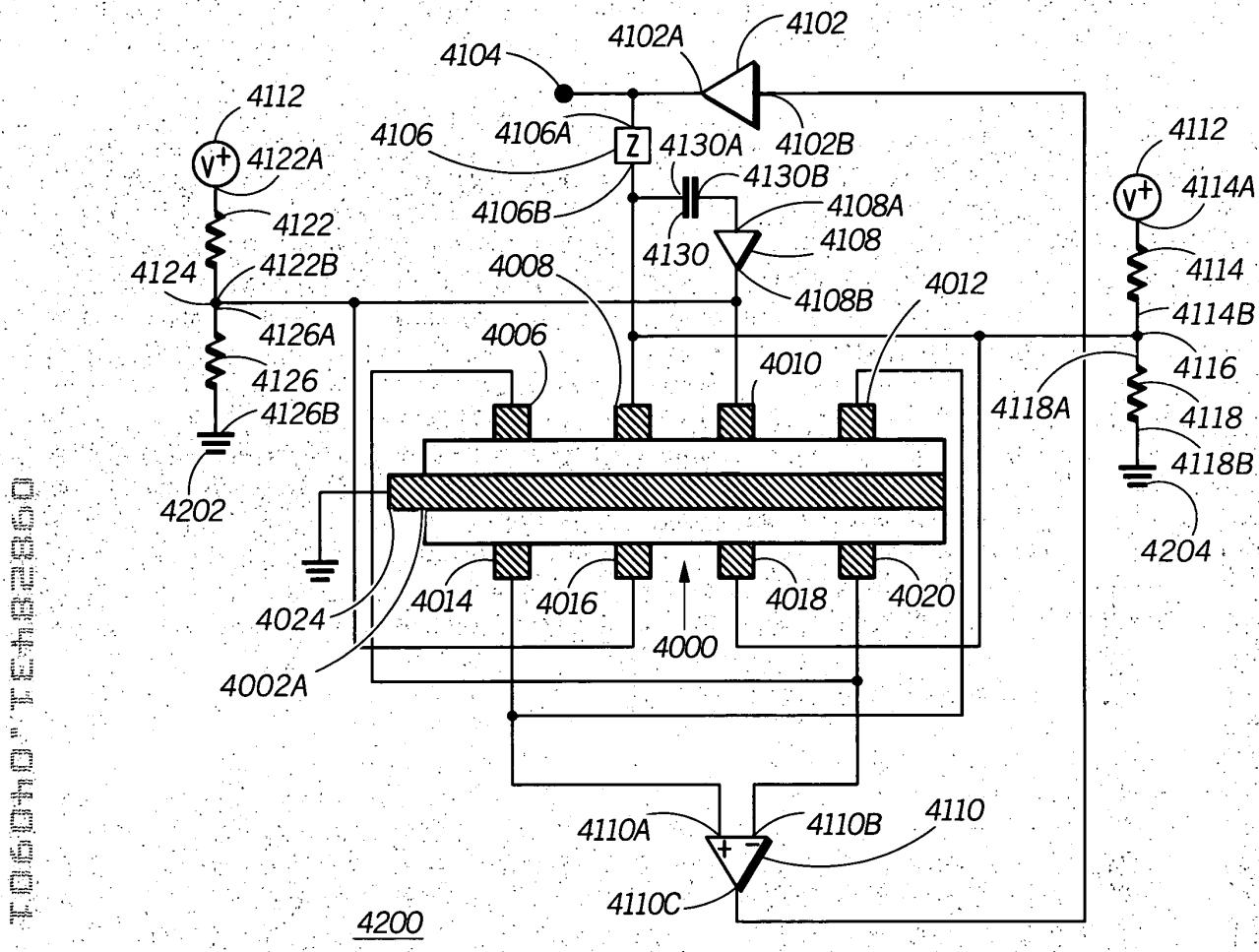


FIG. 42